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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants:	Daniel L. Auclair et al.		
Title:	Soft Errors Handling in EEprom Devices		
Application No.:	08/908,265	Filing Date:	August 7, 1997
Examiner:	Moise, Emmanuel Lionel	Group Art Unit:	2133
Docket No.:	M-10202-3C US	Conf. No.:	9300

San Francisco, California
January 29, 2003

Commissioner for Patents
Washington, D. C. 20231

RESPONSE

Dear Sir:

These remarks are in response to the to the Official Action mailed on October 30, 2002. The Office Action rejected all of the pending claims, claims 35, 36, 38-40, and 45-51 under 35 U.S.C. 102(b) based on U.S. patent number 4,827,450 of Kowalski. These rejections are respectfully submitted to be in error.

As noted in the Office Action, claim 35 was copied from U.S. patent number 5,652,720 for proposes of an interference, as were claims 36, 40, and, in modified form, claims 38 and 39. It is respectfully submitted that this rejection is improper as the grounds for rejection of the present application under 35 U.S.C. 102(b) would also be applicable to the patent from which the claims were copied. Any such rejection is required to have the approval of the Group Director, which is not found included in the present Office Action. Consequently, the rejection of claims 35, 36, and 38-40 must be with drawn on this basis alone. (Cf. M.P.E.P. § 2307.02 and § 1003.)

Additionally, it is also believed that the basis of the rejection itself is not well founded. U.S. patent number 4,827,450 of Kowalski presents a device for determining if a EEPROM memory has been subjected to too high a supply voltage, as described at column 1, lines 45-68. This is done by providing a special cell (referred to as a "warning cell" CO) that is

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programmed into a special state (column 2, lines 10-13 and 51-60). This arrangement does not tell if a memory cell, and in particular the distinguished non-data storing warning cell, has degraded, but only if the memory has been subjected to an excessive read voltage. As described beginning at column 3, line 42, this accomplished by *simultaneously* (and continuously) applying a *single* voltage (V_{CC}) to *multiple* terminals of the special cell (the drain and control gate of transistor T_1, as well a E2 for the p-channel $V_{ref}=V_{CC}$ case). The result of this arrangement is a warning from the warning cell if too high a read voltage has been applied, which in turn may possibly be a cause of a read related disturb in the actual data storing memory cells.

Thus, the device of Kowalski describes *simultaneously* applying a *single* voltage to a *plurality* of terminals to generate a *single*, continuous read result. This is quite distinction from the device of the present invention as presented in the claims, where *multiple* voltages are applied to a *single terminal* to generate *more than one* read result. This distinction is reflected in the claims. For example, the second element of claim 35 states:

> means for determining a likelihood that the memory device has a degraded state by applying each of *a plurality of read voltages* to *a terminal* of a first cell of the plurality of memory cells to generate *a plurality of read results*.

As the added emphasis shows, this is quite distinct from the cited reference. These distinctions are also present in the other independent claim, claim 45:

> applying said first read voltage to a terminal of a first cell ...;
> generating a first read result in response ...;
> applying said second read voltage to said terminal of said first cell;
> generating a second read result in response ... .

Consequently, it is respectfully submitted that the rejection of independent claims 35 and 45, along with that of dependent claims 36, 38-40, and 45-51, is not well founded and should be withdrawn.

Dependent claims 36, 38-40, and 45-51 are all believed to be further allowable based on additional reasons; however, as no specific rejection of these claims were presented in the Office Action, these additional reasons for their allowability will not be presented here in order to save space.

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For any of these reasons, the rejection of the pending claims is respectfully submitted to be in error. Reconsideration of the Office Action's rejection of claims 35, 36, 38-40, and 45-51, and a prompt declaration of their allowability is respectfully requested.

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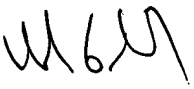
Respectfully submitted,



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APPENDIX

Pending claims

35. A memory device comprising:

a plurality of memory cells, each of which is readable by application of a read voltage; and

means for determining a likelihood that the memory device has a degraded state by applying each of a plurality of read voltages to a terminal of a first cell of the plurality of memory cells to generate a plurality of read results.

36. The memory device of claim 35, wherein a group of the plurality of memory cells are arranged in a row that includes the cell, the memory device further comprising means for rewriting a previously stored value into each of the group of memory cells when the means for determining determines that the first cell has a degraded state.

(Claim 37 has been cancelled.)

38. The memory device of claim 35, wherein:

a group of the plurality of memory cells are arranged in a row that includes the first cell; and

the means for determining includes means for determining the likelihood by applying each of the plurality of read voltages when a write is performed on the group of memory cells.

39. The memory device of claim 35, wherein:

a group of the plurality of memory cells are arranged in a row that includes the first cell; and

the means for determining includes means for determining the likelihood by applying each of the plurality of read voltages when a read is performed on the group of memory cells.

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40. The memory device of claim 35, wherein the terminal of the first cell is a control gate terminal of the first cell.

(Claims 41-44 have been cancelled.)

45. A method of operating a memory device having a plurality of memory cells, comprising:

generating a first read voltage;

applying said first read voltage to a terminal of a first cell of the plurality of memory cells;

generating a first read result in response to said applying said first read voltage;

generating a second read voltage;

applying said second read voltage to said terminal of said first cell;

generating a second read result in response to said applying said first read voltage; and

determining from said first and second read results whether data storage of the memory device is deteriorated.

46. The method of claim 45, further comprising:

rewriting data to said plurality of memory cells in response to determining from said first and second read results that the data storage of the memory device is deteriorated.

47. The method of claim 46, wherein the data values written into said plurality of memory cells in said rewriting are determined based on error correction code (ECC).

48. The method of claim 45, wherein said method is part of a programming process.

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49. The method of claim 45, wherein said method is part of a reading process.

50. The method of claim 45, wherein said memory cells are multi-state memory cells.

51. The method of claim 45, wherein said memory cells are floating gate transistors and said terminal is a control gate.

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